

INA121

FET-Input, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW BIAS CURRENT:** $\pm 4\text{pA}$
- **LOW QUIESCENT CURRENT:** $\pm 450\mu\text{A}$
- **LOW INPUT OFFSET VOLTAGE:** $\pm 200\mu\text{V}$
- **LOW INPUT OFFSET DRIFT:** $\pm 2\mu\text{V}/^\circ\text{C}$
- **LOW INPUT NOISE:**
 $20\text{nV}/\sqrt{\text{Hz}}$ at $f = 1\text{kHz}$ ($G = 100$)
- **HIGH CMR:** 106dB
- **WIDE SUPPLY RANGE:** $\pm 2.25\text{V}$ to $\pm 18\text{V}$
- **LOW NONLINEARITY ERROR:** 0.001% max
- **INPUT PROTECTION TO $\pm 40\text{V}$**
- **8-PIN DIP AND SO-8 SURFACE MOUNT**

APPLICATIONS

- **LOW-LEVEL TRANSDUCER AMPLIFIERS**
Bridge, RTD, Thermocouple
- **PHYSIOLOGICAL AMPLIFIERS**
ECG, EEG, EMG, Respiratory
- **HIGH IMPEDANCE TRANSDUCERS**
- **CAPACITIVE SENSORS**
- **MULTI-CHANNEL DATA ACQUISITION**
- **PORTABLE, BATTERY OPERATED SYSTEMS**
- **GENERAL PURPOSE INSTRUMENTATION**

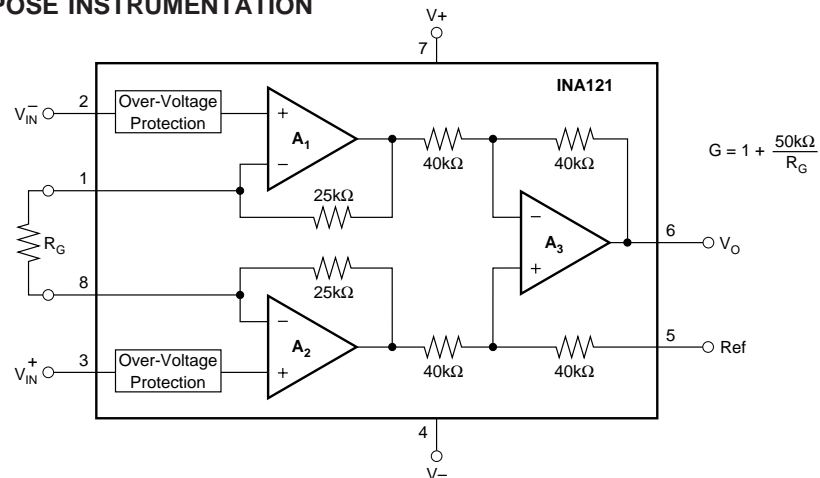
DESCRIPTION

The INA121 is a FET-input, low power instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and very small size make it ideal for a variety of general purpose applications. Low bias current ($\pm 4\text{pA}$) allows use with high impedance sources.

Gain can be set from 1V to 10,000V/V with a single external resistor. Internal input protection can withstand up to $\pm 40\text{V}$ without damage.

The INA121 is laser-trimmed for very low offset voltage ($\pm 200\mu\text{V}$), low offset drift ($\pm 2\mu\text{V}/^\circ\text{C}$), and high common-mode rejection (106dB at $G = 100$). It operates on power supplies as low as $\pm 2.25\text{V}$ ($+4.5\text{V}$), allowing use in battery operated and single 5V systems. Quiescent current is only $450\mu\text{A}$.

Package options include 8-pin plastic DIP and SO-8 surface mount. All are specified for the -40°C to $+85^\circ\text{C}$ industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = \pm 15V$

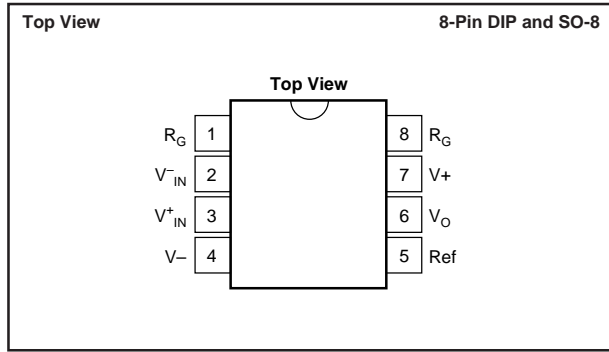
At $T_A = +25^\circ C$, $V_S = \pm 15V$, $R_L = 10k\Omega$, and I_A reference = $0V$, unless otherwise noted.

PARAMETER	CONDITIONS	INA121P, U			INA121PA, UA			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT									
Offset Voltage, RTI vs Temperature	$V_S = \pm 2.25V$ to $\pm 18V$		$\pm 200 \pm 200/G$	$\pm 500 \pm 500/G$		$\pm 300 \pm 200/G$	$\pm 1000 \pm 1000/G$	μV $\mu V/^\circ C$	
vs Power Supply			$\pm 2 \pm 2/G$	$\pm 5 \pm 20/G$		*	$\pm 15 \pm 20/G$	$\mu V/V$	
Long-Term Stability			$\pm 5 \pm 20/G$	$\pm 50 \pm 150/G$		*	*	$\mu V/mo$	
Impedance, Differential	$V_O = 0V$		± 0.5			*		$\Omega \parallel pF$	
Common-Mode			$10^{12} \parallel 1$	$10^{12} \parallel 12$		*		$\Omega \parallel pF$	
Input Voltage Range	$V_{CM} = -12.5V$ to $13.5V$		See Text and Typical Curves			*			
Safe Input Voltage				± 40		*	*	V	
Common-Mode Rejection		$G = 1$	78	86		72	*		dB
		$G = 10$	91	100		85	*		dB
	$G = 100$	96	106		90	*		dB	
	$G = 1000$		106			*		dB	
BIAS CURRENT	$V_{CM} = 0V$		± 4	± 50		*	*	pA	
vs Temperature			See Typical Curve			*			
Offset Current			± 0.5			*		pA	
vs Temperature			See Typical Curve			*			
NOISE, RTI	$R_S = 0\Omega$								
Voltage Noise: $f = 10Hz$	$G = 100$		30			*		nV/\sqrt{Hz}	
$f = 100Hz$	$G = 100$		21			*		nV/\sqrt{Hz}	
$f = 1kHz$	$G = 100$		20			*		nV/\sqrt{Hz}	
$f = 0.1Hz$ to $10Hz$	$G = 100$		1			*		$\mu Vp-p$	
Current Noise: $f = 1kHz$			1			*		fA/\sqrt{Hz}	
GAIN									
Gain Equation	$V_O = -14V$ to $13.5V$	1	$1 + (50k\Omega/R_G)$			*	*	V/V	
Range of Gain				10,000		*	*	V/V	
Gain Error		$G = 1$		± 0.01	± 0.05		*	± 0.1	%
		$G = 10$		± 0.03	± 0.4		*	± 0.5	%
		$G = 100$		± 0.05	± 0.5		*	± 0.7	%
	$G = 1000$		± 0.5			*	%		
Gain vs Temperature ⁽¹⁾	$G = 1$		± 1	± 10		*	*	ppm/ $^\circ C$	
	$G > 1$		± 25	± 100		*	*	ppm/ $^\circ C$	
Nonlinearity	$V_O = -14V$ to $13.5V$					*		% of FSR	
	$G = 1$		± 0.0002	± 0.001		*	± 0.002	% of FSR	
	$G = 10$		± 0.0015	± 0.005		*	± 0.008	% of FSR	
	$G = 100$		± 0.0015	± 0.005		*	± 0.008	% of FSR	
	$G = 1000$		± 0.002			*		% of FSR	
OUTPUT									
Voltage: Positive	$R_L = 100k\Omega$		$(V+) - 0.9$			*		V	
Negative	$R_L = 100k\Omega$		$(V-) + 0.15$			*		V	
Positive	$R_L = 10k\Omega$	$(V+) - 1.5$	$(V+) - 0.9$		*	*		V	
Negative	$R_L = 10k\Omega$	$(V-) + 1$	$(V-) + 0.25$		*	*		V	
Capacitance Load Drive			1000			*		pF	
Short-Circuit Current			± 14			*		mA	
FREQUENCY RESPONSE									
Bandwidth, -3dB	$G = 1$		600			*		kHz	
	$G = 10$		300			*		kHz	
	$G = 100$		50			*		kHz	
	$G = 1000$		5			*		kHz	
Slew Rate	$V_O = \pm 10V$, $G \leq 10$		0.7			*		V/ μs	
Settling Time, 0.01%	$G = 1$ to 10		20			*		μs	
	$G = 100$		35			*		μs	
	$G = 1000$		260			*		μs	
Overload Recovery	50% Input Overload		5			*		μs	
POWER SUPPLY									
Voltage Range		± 2.25	± 15	± 18	*	*	*	V	
Quiescent Current	$I_O = 0V$		± 450	± 525		*	*	μA	
TEMPERATURE RANGE									
Specification		-40		85	*		*	$^\circ C$	
Operating		-55		125	*		*	$^\circ C$	
Storage		-55		125	*		*	$^\circ C$	
Thermal Resistance, θ_{JA}									
8-Lead DIP			100			*		$^\circ C/W$	
SO-8 Surface Mount			150			*		$^\circ C/W$	

* Specification same as INA121P, U.

NOTE: (1) Temperature coefficient of the "Internal Resistor" in the gain equation. Does not include TCR of gain-setting resistor, R_G .

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	$\pm 18V$
Analog Input Voltage Range	$\pm 40V$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	$-55^{\circ}C$ to $+125^{\circ}C$
Storage Temperature	$-55^{\circ}C$ to $+125^{\circ}C$
Junction Temperature	$+150^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

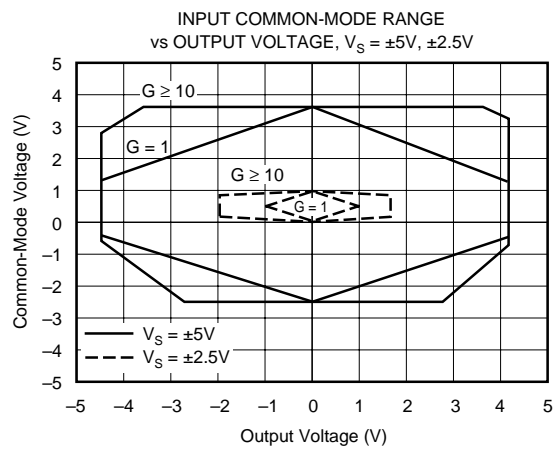
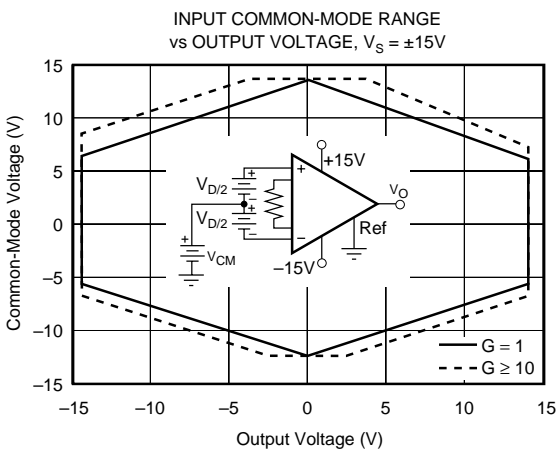
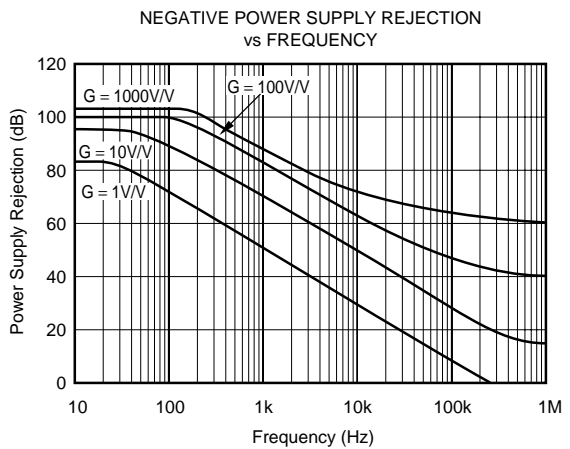
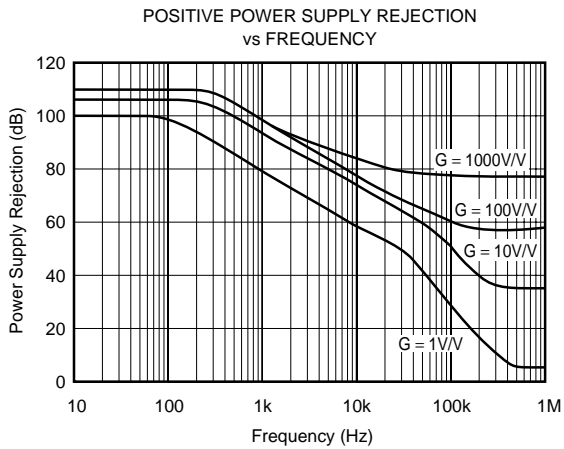
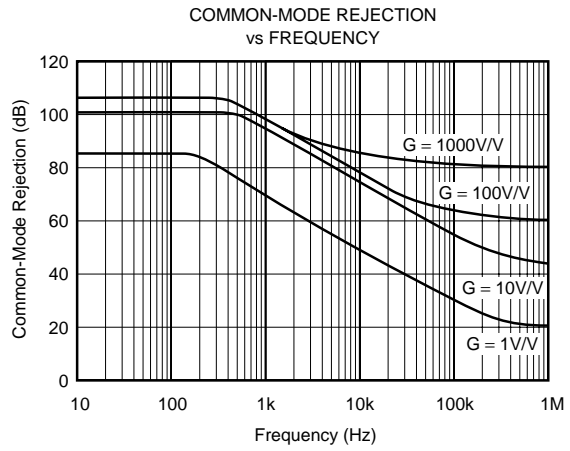
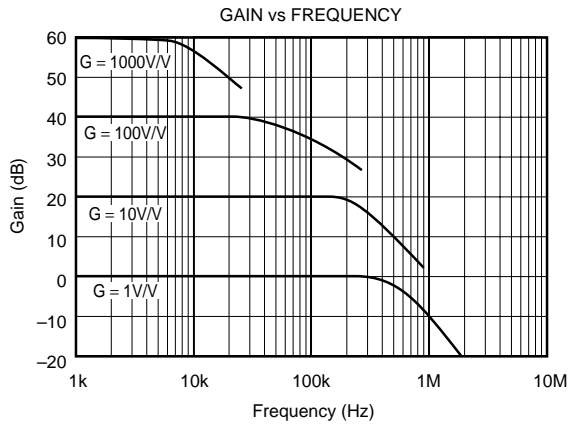
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
Single						
INA121P	8-Pin DIP	006	$-40^{\circ}C$ to $+85^{\circ}C$	INA121P	INA121P	Rails
INA121PA	8-Pin DIP	006	$-40^{\circ}C$ to $+85^{\circ}C$	INA121PA	INA121PA	Rails
INA121U	SO-8 Surface-Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$	INA121U	INA121U	Rails
"	"	"	"	"	INA121U/2K5	Tape and Reel
INA121UA	SO-8 Surface-Mount	182	$-40^{\circ}C$ to $+85^{\circ}C$	INA121UA	INA121UA	Rails
"	"	"	"	"	INA121UA/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA121U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

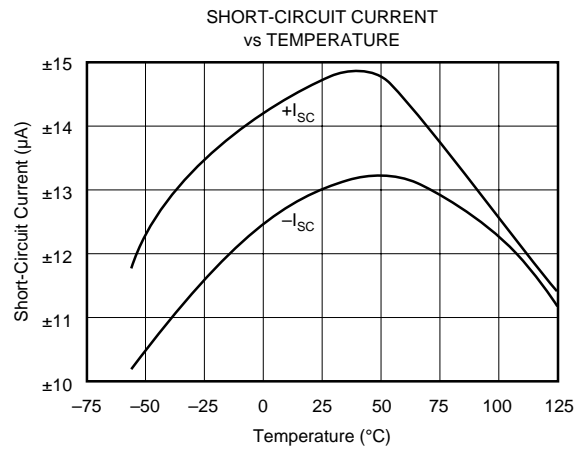
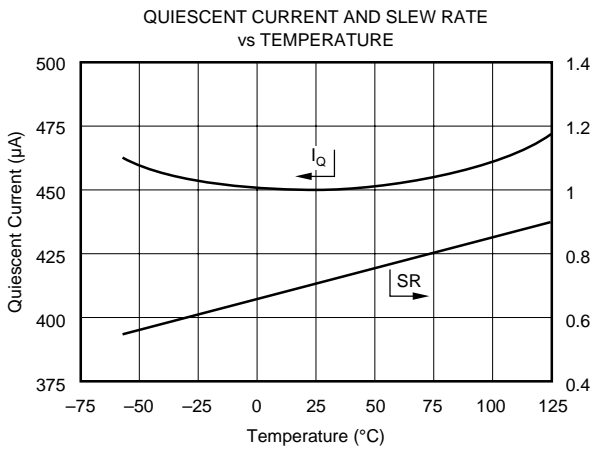
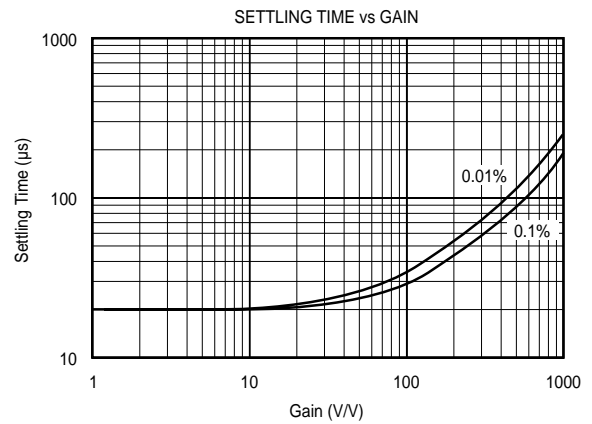
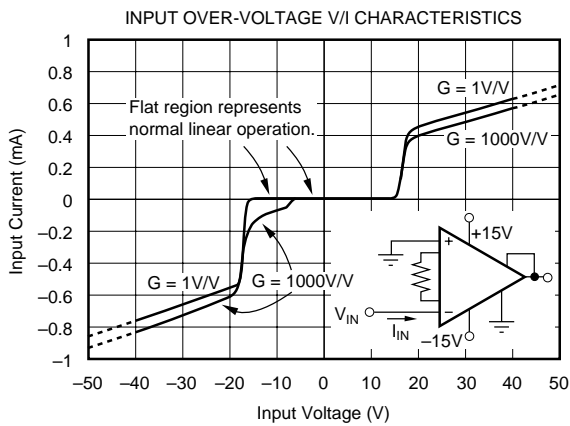
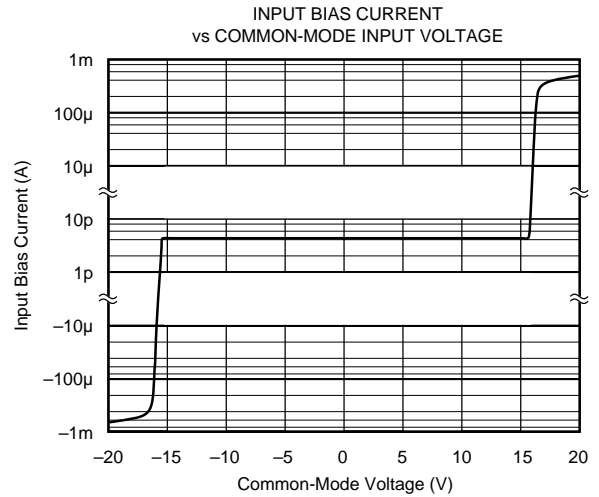
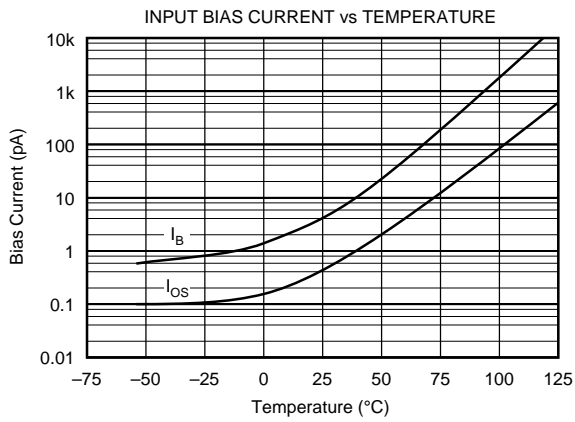
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



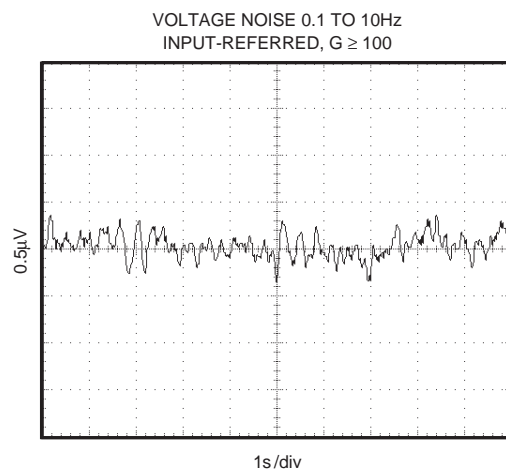
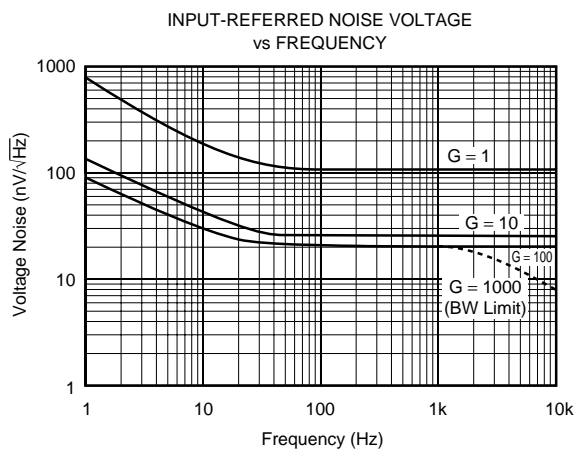
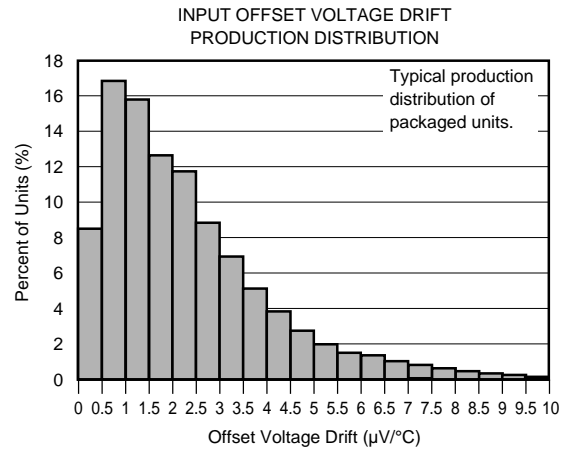
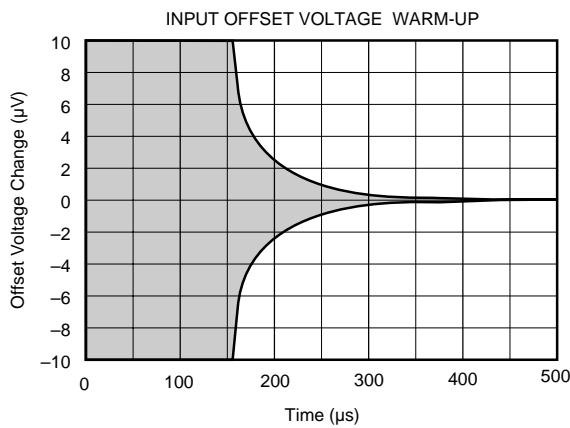
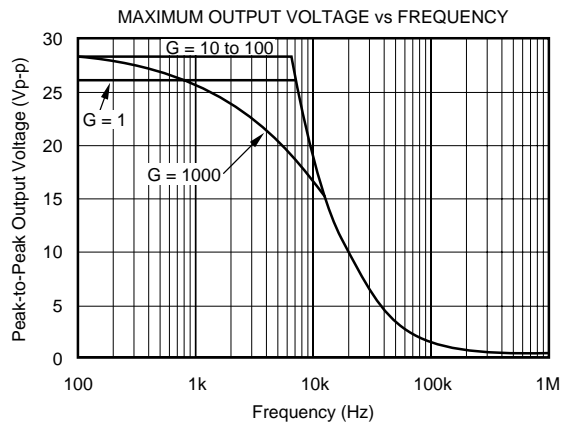
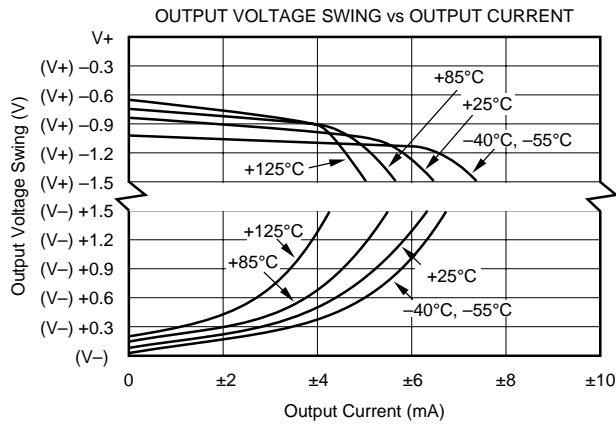
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



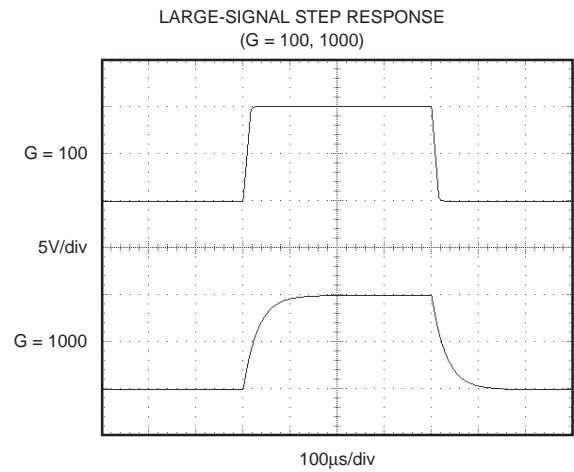
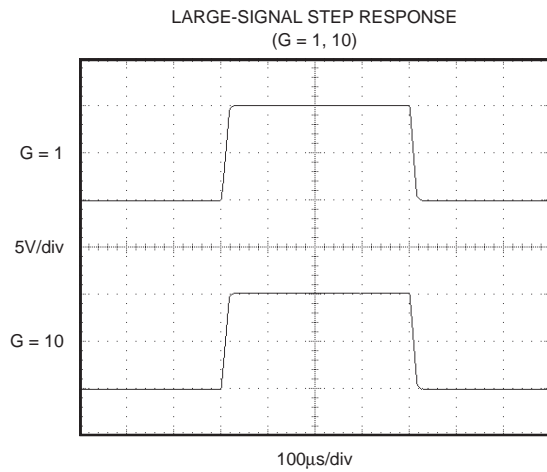
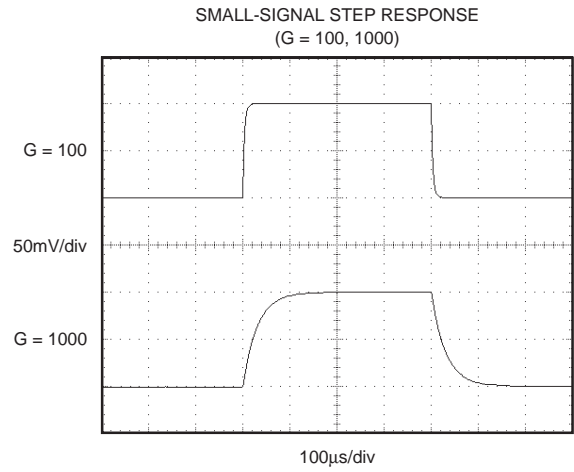
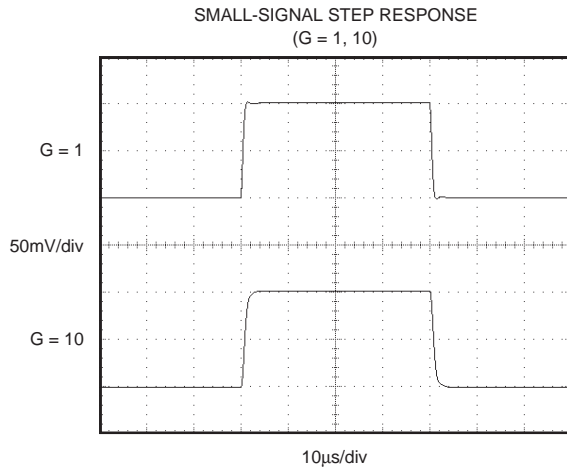
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA121. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ($G = 1$).

SETTING THE GAIN

Gain of the INA121 is set by connecting a single external resistor, R_G , connected between pins 1 and 8:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2 . These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA121.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA121 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA121. Settling time also remains excellent at high gain.

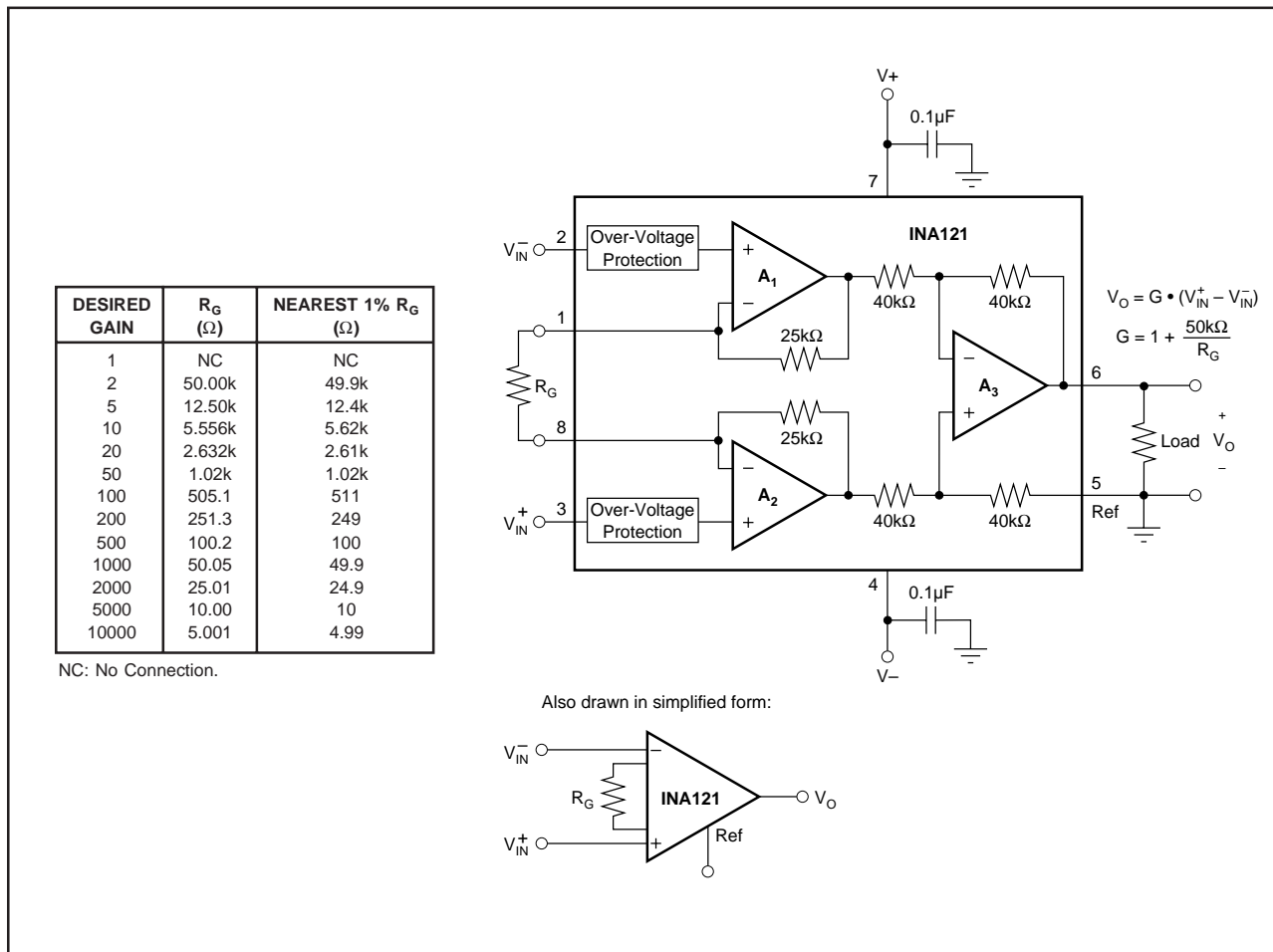


FIGURE 1. Basic Connections.

The INA121 provides excellent rejection of high frequency common-mode signals. The typical performance curve, “Common-Mode Rejection vs Frequency” shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the V_{IN}^+ and V_{IN}^- connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

NOISE AND ACCURACY PERFORMANCE

The INA121’s FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2k Ω to 50k Ω the INA114, INA128, or INA129 may provide lower offset voltage and drift. For very low source impedance ($\leq 1k\Omega$), the INA103 may provide improved accuracy and lower noise. At very high source impedances ($> 1M\Omega$) the INA116 is recommended.

OFFSET TRIMMING

The INA121 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

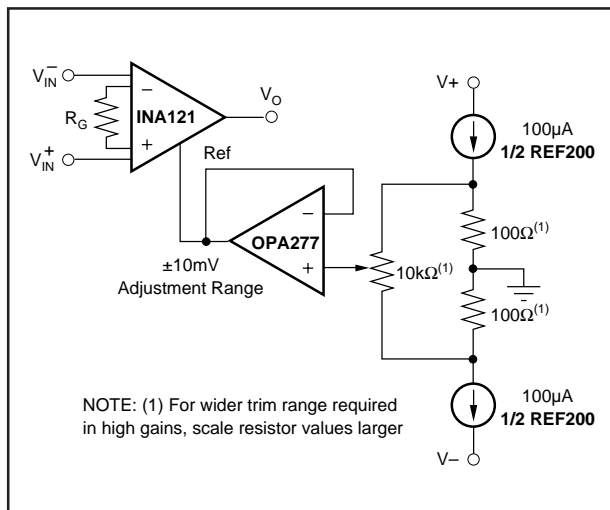


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA121 is extremely high—approximately $10^{12}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 4pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA121 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA121 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

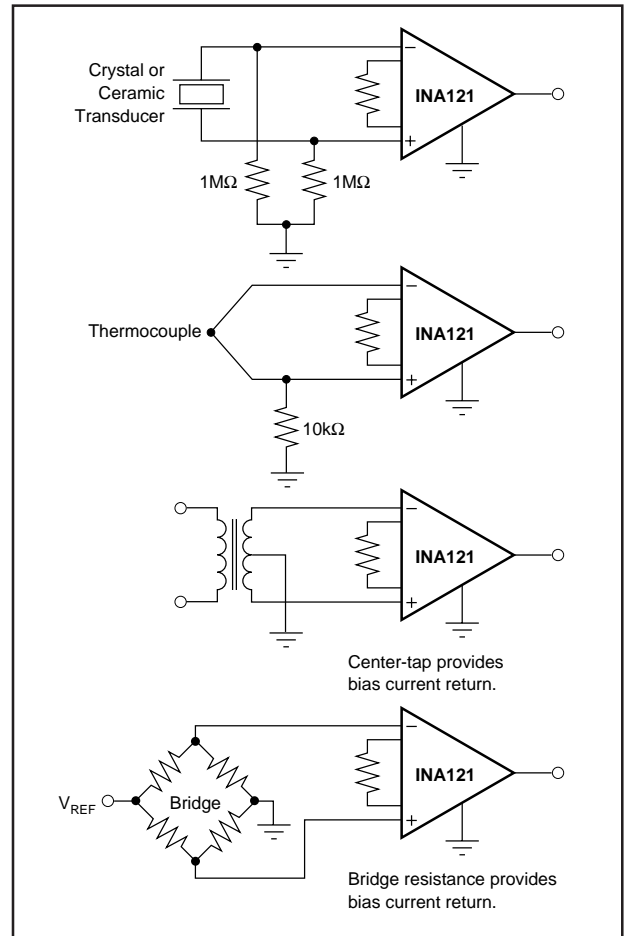


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA121 is from approximately 1.2V below the positive supply voltage to 2.1V above the negative supply. A differential input voltage causes the output voltage to increase. The linear input range, however, will be limited by the output voltage swing of amplifiers A_1 and A_2 . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see typical performance curve “Input Common-Mode Range vs Output Voltage”.

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA121 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA121 to increase the voltage swing.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A_3 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA121 can be operated on power supplies as low as $\pm 2.25V$. Performance remains excellent with power supplies ranging from $\pm 2.25V$ to $\pm 18V$. Most parameters vary only slightly throughout this supply voltage range—see typical

performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage” show the range of linear operation for $\pm 15V$, $\pm 5V$, and $\pm 2.5V$ supplies.

INPUT FILTERING

The INA121’s FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 5 shows proper implementation of this input filter to preserve the INA121’s excellent high frequency common-mode rejection. Mismatch of the common-mode input time constant (R_1C_1 and R_2C_2), either from stray capacitance or mismatched values, causes a high frequency common-mode signal to be converted to a differential signal. This degrades common-mode rejection. The differential input capacitor, C_3 , reduces the bandwidth and mitigates the effects of mismatch in C_1 and C_2 . Make C_3 much larger than C_1 and C_2 . If properly matched, C_1 and C_2 also improve ac CMR.

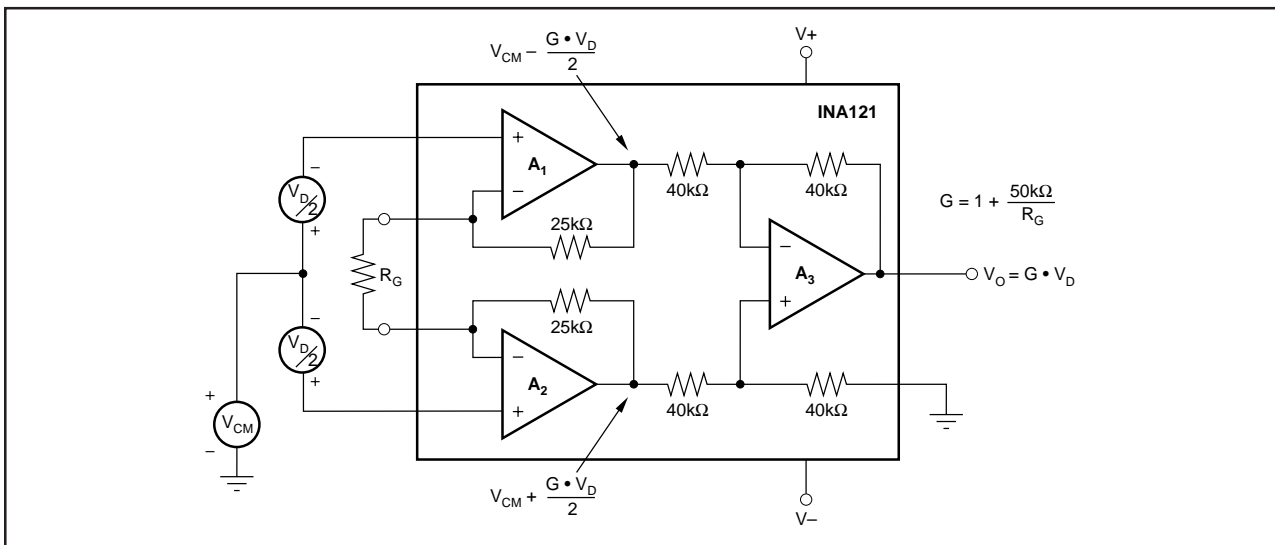


FIGURE 4. Voltage Swing of A_1 and A_2 .

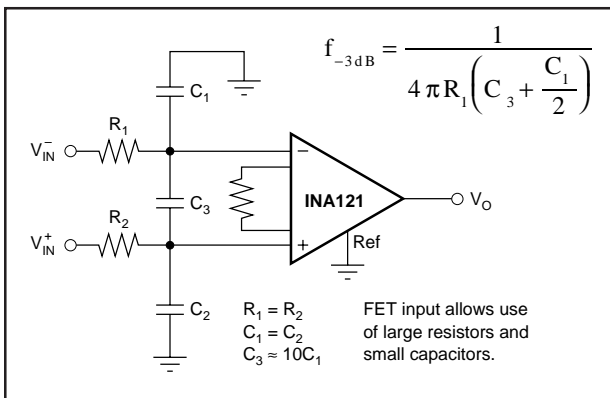


FIGURE 5. Input Low-Pass Filter.

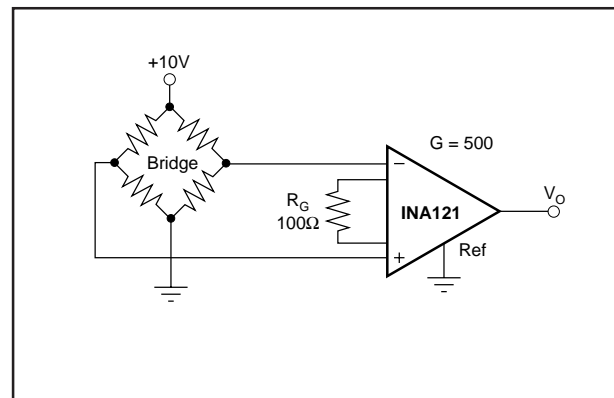


FIGURE 6. Bridge Transducer Amplifier.

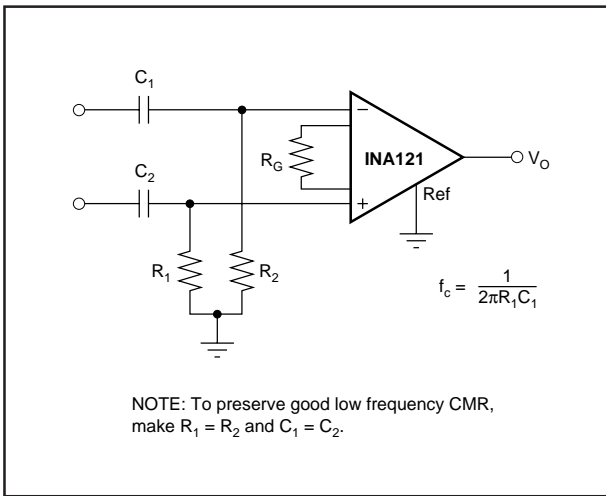


FIGURE 7. High-Pass Input Filter.

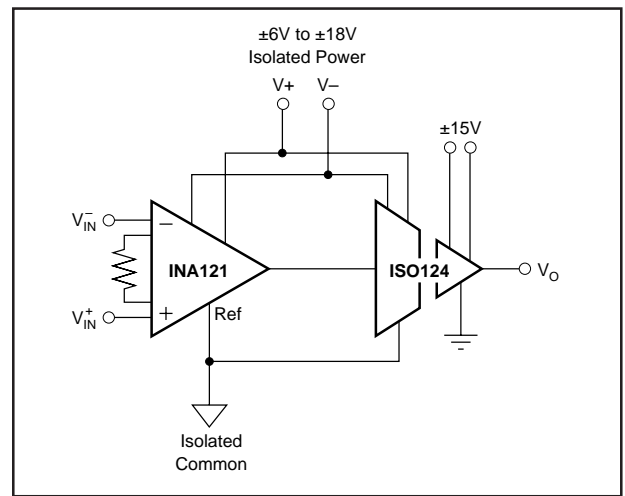


FIGURE 8. Galvanically Isolated Instrumentation Amplifier.

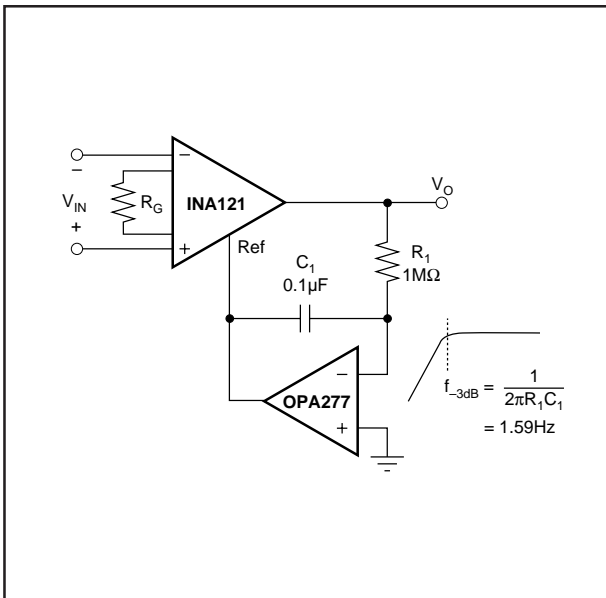


FIGURE 9. AC-Coupled Instrumentation Amplifier.

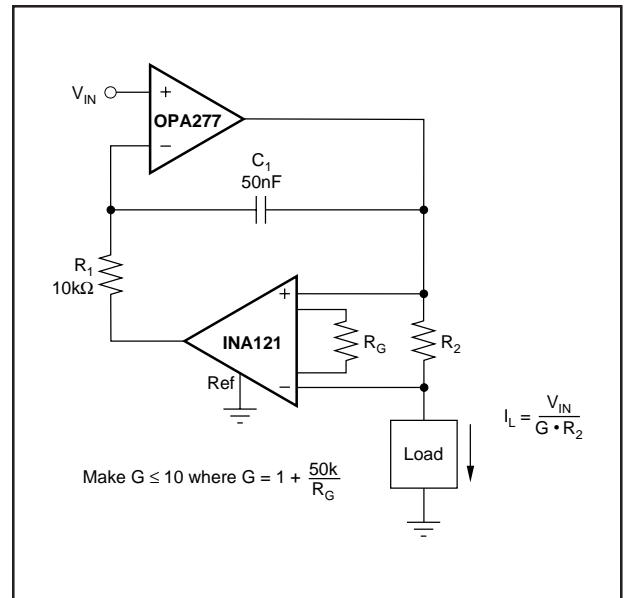


FIGURE 10. Voltage Controlled Current Source.

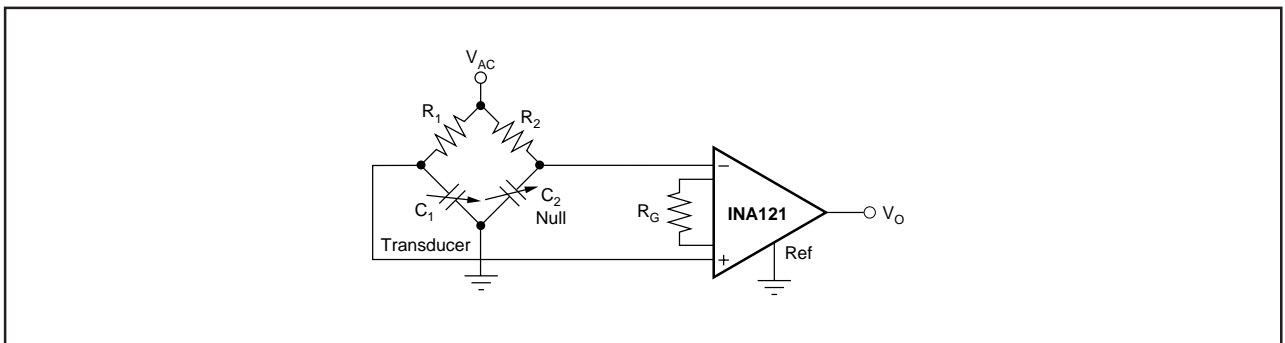


FIGURE 11. Capacitive Bridge Transducer Circuit.

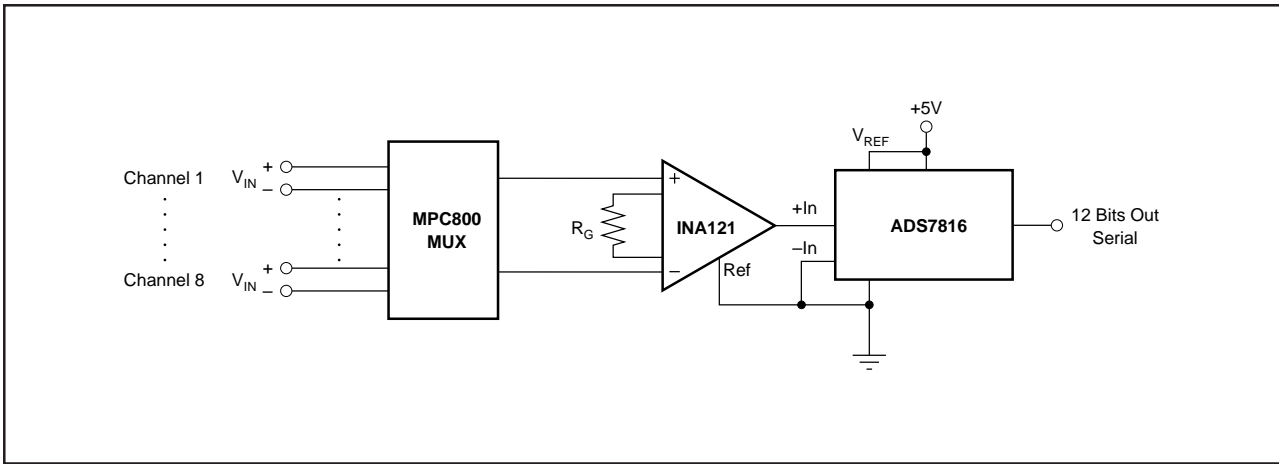


FIGURE 12. Multiplexed-Input Data Acquisition System.

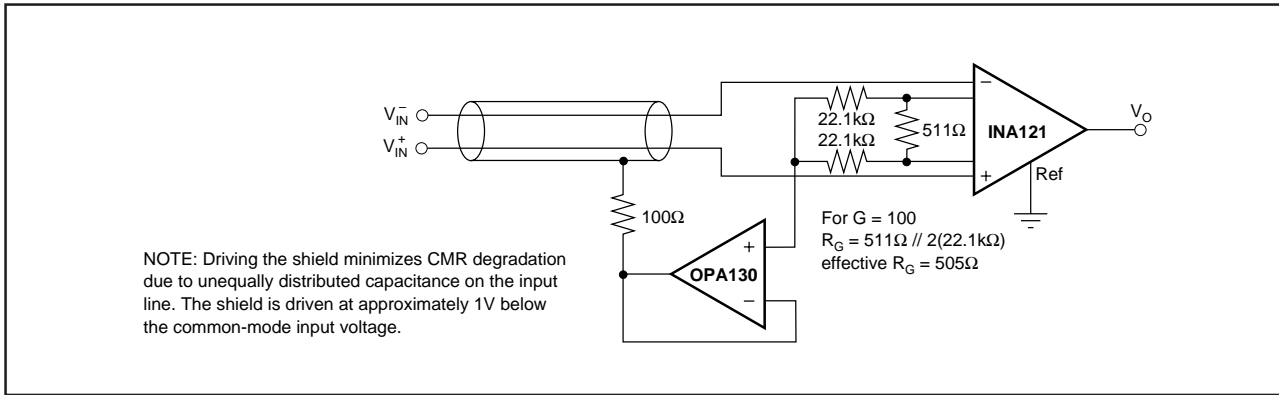


FIGURE 13. Shield Driver Circuit.

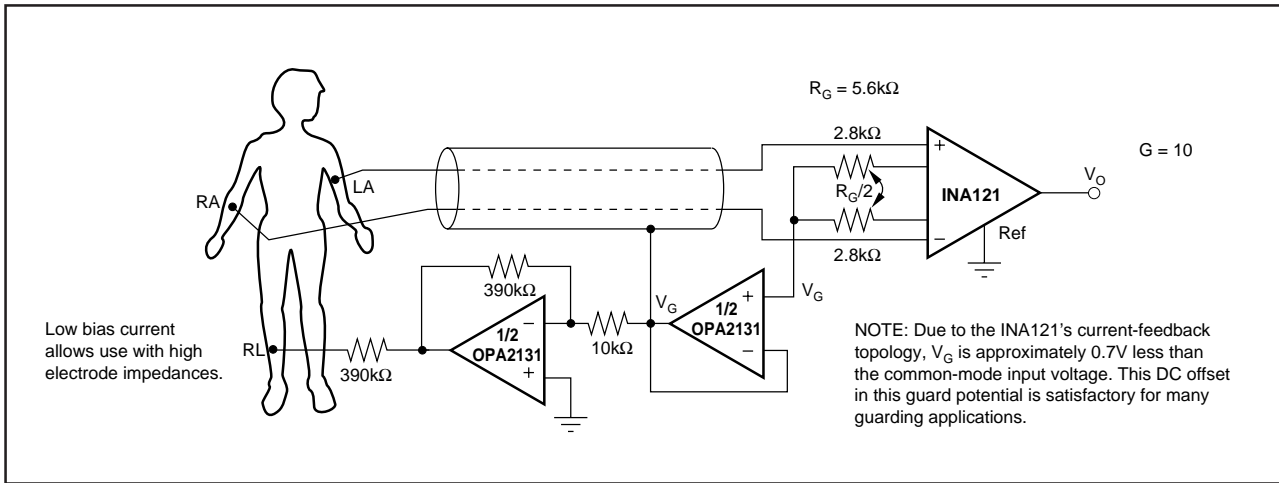


FIGURE 14. ECG Amplifier With Right-Leg Drive.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
INA121P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA121PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA121PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA121PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA121U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA121UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA121U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA121UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA121U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
INA121UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated